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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,811	01/14/2004	Jeffrey P. Gambino	BUR920020121US1	1810

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EXAMINER	
GURLEY, LYNNE ANN	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,811	GAMBINO ET AL.	
	Examiner	Art Unit	
	Lynne A. Gurley	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment with remarks filed 4/5/06.

Currently, claims 1-3 and 5-9 are pending.

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. The rejection of claims 1-3 and 5-9 under 35 U.S.C. 102(e) as being anticipated by Babich et al. (US 6,815,329, dated 11/9/04, filed 4/2/02) has been maintained for the reasons of record.

Babich shows the method as claimed in figures 3-7 and corresponding text as a method of forming an interconnect structure comprising the steps of: providing a lower metal wiring layer having first metal lines located within a lower low-k dielectric (fig. 5, level 250); depositing an upper low-k dielectric 280 atop the lower metal wiring layer; etching at least one portion of the

upper low-k dielectric to provide at least one via to the first metal lines; forming rigid dielectric sidewall spacers (fig. 4; column 4, lines 61-67; column 5, lines 1-19 and lines 20-50 for the material of the sidewall; column 6, lines 11-14) in the at least one via of the upper low-k dielectric, the dielectric sidewall spacers are of a material selected from the group consisting of SiCH, SiCOH, SiC and SiO2 (column 5, lines 1-19 and lines 20-50; column 6, lines 11-14); and forming second metal lines in the at least one portion of the upper low-k dielectric. The upper and lower low-k dielectric has a dielectric constant ranging from about 1.0 to about 3.5 and comprise low-k polymers or low-k carbon doped oxides. Processes for forming the rigid dielectric sidewall spacers are given (column 5, lines 51-57). A rigid insulating layer has been deposited atop the lower low-k dielectric and the lower wiring layer (fig. 5).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-3 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chooi et al. (US 6,284,657, dated 9/4/01) in view of Babich et al. (US 6,815,329, dated 11/9/04, filed 4/2/02).

Chooi shows the method as claimed in figures 4-14 and corresponding text, with a method of forming an interconnect structure comprising the steps of: providing a lower metal wiring layer having first metal lines 10; depositing an upper low-k dielectric 14/18 atop the lower metal wiring layer; etching at least one portion of the upper low-k dielectric to provide at least one via 24 to the first metal lines (fig. 2); forming rigid dielectric sidewall spacers 15/19 (SiC; figs. 5-6; column 6, lines 21-32) in the at least one via of the upper low-k dielectric, the dielectric sidewall spacers are of a material selected from the group consisting of SiCH, SiCOH, SiC and SiO2; and forming second metal lines in the at least one portion of the upper low-k dielectric (column 7, lines 4-7). The upper low-k dielectric has a dielectric constant ranging from about 1.0 to about 3.5 and comprise low-k polymers or low-k carbon doped oxides (column 5, lines 21-43). Processes for forming the rigid dielectric sidewall spacers are given (CVD,

PVD, 50-5000 Angstroms, anisotropic etch; column 6, lines 21-50). A rigid insulating layer has been deposited atop the lower metal wiring layer (Si3N4 or BLOK; column 7, lines 58-60).

Chooi lacks anticipation only in not teaching that: 1? The spacers are SiCH, SiCOH or SiO2; 2) the first metal line is located within a lower low-k dielectric; 3) the lower low-k dielectric have a dielectric constant ranging from about 1.0 to about 3.5 and comprise low-k polymers or low-k carbon doped oxides; and 4) the lower metal wiring layer further comprises a rigid insulating layer deposited atop the lower low-k dielectric.

Babich teaches that in a multilayer interconnect structure, there are multiple levels of the damascene structure, in which the vias and interconnect lines are embedded in low-k dielectrics such as air gap or low-k polymers or low-k carbon doped oxides. Dielectric spacers are used from the group consisting of SiCH, SiCOH and SiO2 (column 6, lines 11-18; column 5, lines 20-50).

It would have been obvious to one of ordinary skill in the art to have located the first metal line within a lower low-k dielectric; 2) to have had the lower low-k dielectric have a dielectric constant ranging from about 1.0 to about 3.5 and comprise low-k polymers or low-k carbon doped oxides; and 3) to have had the lower metal wiring layer further comprises a rigid insulating layer deposited atop the lower low-k dielectric, in the method of Chooi, with the motivation given from Babich that multilayered interconnects, which would comprise a plurality of the structures shown in Chooi, would be embedded in low-k dielectrics and, using the dielectric spacer technology including the materials selected from the group consisting of SiCH, SiCOH and SiO2, in order to reduce the parasitic capacitance and improve overall performance of the device.

Response to Arguments

8. Applicant's arguments filed 4/5/06 have been fully considered but they are not persuasive. In response to Applicant's remarks concerning Babich not showing the solid sidewall spacer material, the Examiner notes that Babich defines the purpose of the dielectric sidewall spacers in column 4, lines 12-25 and also notes that the description of the solid dielectrics in column 5 is general, when taken from the broadest interpretation of the reference. This reading is reasonable in that the materials listed in column 5 as the solid dielectrics are fully capable of performing the key functions of the dielectric sidewall spacers in column 4.

9. Additionally, in response to the rejection made under Chooi in view of Babich. Since SiC is used in Chooi for the spacers, it would be obvious to one of ordinary skill in the art to substitute the materials which are SiC variations taught in Babich for the SiC in Chooi.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See the PTO Form 892.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

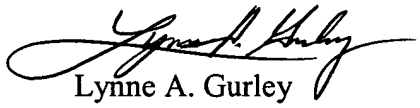
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is 571-272-1670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lynne A. Gurley
Primary Patent Examiner
Art Unit 2812

LAG
June 25, 2006